KONRAD JĘDRZEJEWSKI[1], ANATOLIY A. PLATONOV[2,1]

[1]Warsaw University of Technology, Faculty of Electronics and Information Technology,
Poland, e-mail: kala@ise.pw.edu.pl
[2]Moscow Institute of Electronics and Mathematics, Chair of Cybernetics, Russia

ANALYSIS OF INFLUENCE OF INTERNAL CONVERTERS NONLINEARITY ON INTELLIGENT CYCLIC ADC PERFORMANCE*

The task of the paper is the presentation of a modelling approach to quantitative analysis of the influence of internal converter nonlinearities on the performance of sub-optimal intelligent cyclic A/D converters (IC ADCs) developed and analysed in works [1-5] and others. The results of investigations permit to determine requirements to the analogue elements of IC ADC architecture, first of all to an internal low-bit A/D converter (ADC_{In}), which is the most crucial for the design and practical implementation of IC ADC.

Keywords: cyclic A/D converters, nonlinearity of converters, performance

1. INTRODUCTION

Cyclic A/D converters (CADCs) (called also multi-pass, multi-fold, sub-ranging, etc. [6-8]) belong to one of the most widely used classes of A/D converters [6-8]. In works [1-5] and others, the new class of sub-optimal intelligent cyclic A/D converters (IC ADCs) was considered. The principal difference between these and known cyclic converters consists in a transition to the computation of the codes (digital estimates) of input samples, at each cycle of conversion, in the form of long-words of fixed length N_{comp}. Choice of length of the word N_{comp} is conditioned by the required final resolution of the converters (e.g. N_{comp} = 16, 24, 32 bits). In known CADCs the codes are constructed by the cyclic addition of short binary words formed by low-bit (N_{ADC} = 1÷8 bits) internal pre-converter ADC_{In} to result of previous additions (see Sect. 1). Application of long-word arithmetic allows to design the digital part of IC ADCs as the unit permitting to apply highly efficient algorithms [9] to the computation of estimates (codes) of the input signal samples under concurrent adaptive adjusting of the analogue part of the converter.

The objective of the approach developed in [9] and in other works is design of optimal adaptive estimating systems (AES) using mathematical models of the input signals (random processes) and a non-linear model of the analogue part, more adequate than used before. Being applied to IC ADC design, this approach permits to optimize simultaneously the work of their digital and analogue parts [1-5] and to improve their performance as compared to conventional CADC. The advanced mathematical background of the approach permits to develop the efficient software for computer simulations which enables comprehensive numerical analysis, in details, of the particularities of both AES and IC ADC work, including numerical assessment and analysis of their performance.

The results of works [1-4] show a high closeness of numerical assessments of ideal IC ADC characteristics obtained from theoretical calculations and in simulation experiments. This put the

* The work was supported in part by Grant 3 T 11B 059 29 of the Polish Ministry of Science and Information Society Technologies.

basis for application of simulations to the analysis of not only ideal, but also real IC ADCs performance depending on nonlinearities of ADC_{In} in their analogue part. Corresponding experiments can be performed according to the same scheme as used for the analysis of ideal IC ADC. Apart from "natural" step-wise nonlinearity of an ideal ADC_{In} transfer function, its integral and differential nonlinearities are modelled as corresponding transformations of the static model as in Fig. 2. An accurate theoretical investigation of nonlinear effects in actual CADC is an extremely complex task [4] and, for this reason, simulation analysis becomes the important tool in applied research and design of CADC. (It is worth to notice that simulation analysis becomes a more and more widely used tool of analysis of A/D converter function [10]).

The goal of the paper is quantitative and qualitative analysis of the influence of nonlinearities of ADC_{In} on the performance of IC ADC, at each cycle of conversion. Apart from the effective number of bits (ENOB) used in [1-5], the following measures of conversion quality recommended in IEEE Standard [11] are investigated: signal-to-noise and distortion ratio (SINAD) and total harmonic distortion (THD). Until now, the latter measures were not used for analysis of the current performance of IC ADC and CADC. Investigations were carried out using software developed for exact simulation analysis of characteristics of IC ADC with ideal ADC_{In} in the analogue part [1-4].

It is worth to note that in [10, 11] and other fundamental works devoted to ADC modelling and testing, the specific of the cyclic ADC performance assessments is not considered (these converters were considered as “black-box” flash converters). Recent work presents the initial results of researches devoted to the complementation of these works by mathematically grounded model-based methods of assessment of CADC and IC ADC nonlinearities.

2. IC ADC FUNCTIONING PRINCIPLES

A general block diagram of the sub-optimal IC ADC [1-5] is presented in Fig. 1. Each sample $V^{(m)}$ of the input signal is held at the output of the sample-and-hold block (S&H) during the time T sufficient to perform n cycles of conversion. In each k-th cycle ($k=1,...,n$), the computing unit calculates a new estimate (code) $\hat{V}_k^{(m)}$ of the input sample $V^{(m)}$ (each sample is converted in the same way, index m is further omitted).

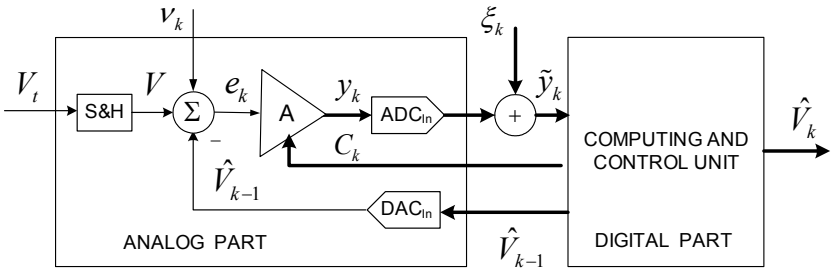

Fig. 1. General architecture of the intelligent cyclic A/D converter.

Codes $\hat{V}_k$ are computed, in each cycle, using a previous estimate $\hat{V}_{k-1}$ stored in the memory unit, and N_{ADC}-bit code ("observation") $\tilde{y}_k$ at the output of pre-converter ADC_{In} according to the relationship common for all CADCs:

$$\hat{V}_k = \hat{V}_{k-1} + L_k \tilde{y}_k, \quad (k = 1, ..., n), \tag{1}$$

$$\tilde{y}_k = C_k e_k + \xi_k, \tag{2}$$

where the values of the coefficients L_k are determined by the algorithm of code $\hat{V}_k$ forming, N_{ADC}-bit codes $\tilde{y}_k$ are the result of conversion of the amplified residual signal $e_k = V - \hat{V}_{k-1} + v_k$ routed to the ADC_{In} input from pre-amplifier (A). Noise ξ_k is the quantization noise whose variance is evaluated according to the commonly used formula $\sigma_\xi^2 = \Delta^2/12 = D^2 \cdot 2^{-2N_{ADC}}/3$, where D = FSR/2 is one half of the full scale range (FSR) of ADC_{In}, and Δ is the ADC_{In} quantization interval. Parameter C_k in (2) describes the gain of amplifier (A), which increases with the number of the conversion cycle. Noise v_k is a summary noise of the feedback D/A converter (DAC_{In}), subtracting block (Σ) and other noise of the analogue part of IC ADC. The form of the static transfer function of an ideal ADC_{In} is presented in Fig.2.

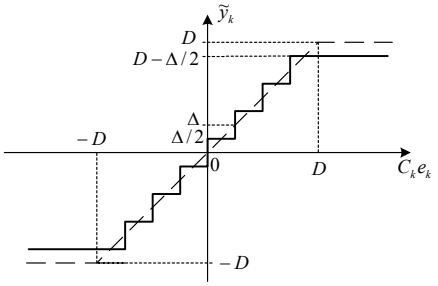

Fig.2. Ideal transfer function of the internal A/D converter ADC_{In}.

The particularity of IC ADC is relinquishment of the binary logic elements used in conventional CADC for the codes $\hat{V}_k$ forming and their computation using a simple long-word (N_{comp} = 16, 24 or 32-bit) computing unit. This unit computes the codes of estimates in the form of N_{comp}-bit binary words according to the Eq. (1). Each new N_{comp}-bit estimate $\hat{V}_k$ is the result of adding the N_{comp}-bit code word $L_k \tilde{y}_k$ to N_{comp}-bit estimate $\hat{V}_{k-1}$ calculated in the previous cycle of conversion. According to [9], optimal values of the gains L_k and C_k which minimize, for each k, the mean square error (MSE) of estimates $P_k = E[(\hat{V}_k - V)^2]$ under a probability of saturation not greater than the given small μ, have the values (see also [1-5]):

$$L_k = \frac{C_k P_k}{\sigma_\xi^2 + C_k^2 \sigma_v^2} = \left(1 - \frac{P_k}{P_{k-1}}\right)\frac{1}{C_k}, \qquad C_k = \frac{D}{\alpha\sqrt{\sigma_v^2 + P_{k-1}}}. \tag{3}$$

In this case, MSE of conversion is calculated according to the formula:

$$P_k = \frac{\sigma_\xi^2 + C_k^2 \sigma_\nu^2}{\sigma_\xi^2 + C_k^2 (\sigma_\nu^2 + P_{k-1})} P_{k-1}. \quad (4)$$

Initial conditions for the algorithm (1)-(4): $\hat{V}_0 = V_0$ and $P_0 = \sigma_0^2$ are determined by the mean value and the maximal power of the input signal. Parameter α in (3) is determined by the accepted probability μ of CADC saturation and satisfies the equation: $\Phi(\alpha) = (1-\mu)/2$, where $\Phi(\alpha)$ is the Gaussian error function. For IC ADC constructed according to the algorithm (1)-(4), the performance of the converter attains the values close to theoretically achievable boundaries established by Eq. (4), (see also [1-4]). This ensures practically full employment of the hardware and software resources for the achievement of maximal resolution and speed of conversion.

3. MODELLING AND ANALYSIS OF NONLINEARITIES INFLUENCE ON IC ADC PERFORMANCE

The transfer function of actual ADC_{In} (referring to the non-ideality of its real characteristic) was modelled on the basis of the ideal transfer function as in Fig.2 with differential and integral nonlinearities (further INL and DNL, respectively). In extension of previous investigations [1-5], where IC ADC performance was analysed using Gaussian and uniformly distributed random test signals, in this work the sine-wave testing signals as well as methods and measures proposed in IEEE Standard [11] were used. Testing sine signals were generated in the form of digital realisations: $V^{(m)} = V_{\max} \sin(2\pi f_0 m)$, $m = (1,...,M)$, where $V_{\max}$ is a half of FSR of IC ADC, and f_0 is the normalized frequency of the test signal. The experiments discussed below were carried for the following values of parameters: M = 1024, f_0 = 53/1024, $V_{\max}$ = 5, V_0 = 0, σ_0 = 1.25, α = 4, D = 1.25, N_{DAC} = 16. It was assumed also that the summary noise v_k at the amplifier input is dominated by the quantization noise of the feedback DAC_{In} and its variance is determined by the relationship $\sigma_\nu^2 = \Delta_{DAC}^2/12 = D_{DAC}^2 2^{-2N_{DAC}}/3$, where N_{DAC} is DAC_{In} resolution. Output range $[-D_{DAC}, D_{DAC}]$ of DAC_{In} is equal to the input range of IC ADC, i.e. $D_{DAC} = V_{\max}$.

A quantitative assessment of the influence of DNL and INL on IC ADC performance was carried out by computing, on the basis of acquired experimental data, the dependencies of ENOB, SINAD and THD on the number of cycles under different intensity of DNL and INL. The assessment of ENOB and SINAD values was performed both in the time and frequency domains [11] (according to [11], assessment in the frequency domain means that corresponding measures are determined from the Discrete Fourier Transform of converted data records).

To evaluate the efficiency of the direct method of ENOB assessment proposed in [12, 13], special series of experiments were also performed. In these experiments, the values of ENOB were estimated as the length of continuous interval of the zeros in the beginning of binary codes of conversion errors $|V^{(m)} - \hat{V}_k^{(m)}|$. This interval determines the number of "true", non-erroneous bits in estimates $\hat{V}_k^{(m)}$ of the samples $V^{(m)}$ of the reference signal. Apart from the measures mentioned above, changes of FFT of the converted signal depending on ADC_{In} nonlinearities and number of cycles were also investigated.

3.1. Differential nonlinearity

The DNL of ADC_{In} transfer function was modelled, similarly to [14], as independent random displacements of each ADC_{In} quantization threshold. The displacements are uniformly distributed around nominal values of thresholds as in Fig.3. The width of the interval $\varepsilon \cdot [-\Delta/2, \Delta/2]$ of possible displacements was set using the scale (intensity) coefficient ε. For large DNL ($\varepsilon > 1$), overlapping of the quantization levels, which cause appearance of missing code errors, may occur.

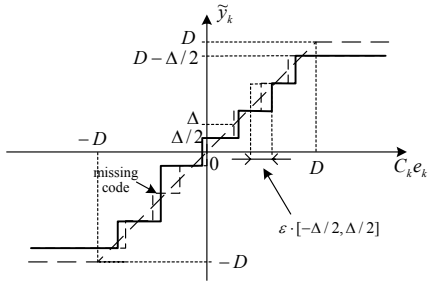

Fig.3. DNL errors model of pre-converter ADC_{In} transfer function.

Fig.4 presents the empirical dependencies of ENOB of IC ADC as a function of cycle number k and different values of intensity of DNL errors ε changed in the interval $0 \le \varepsilon \le 2$. Figures 4 a-c correspond to ENOB assessed under different values of ADC_{In} resolution: N_{ADC} = 2, 4, 8, respectively. These plots were obtained using a "conventional", indirect approach to ENOB measurement based on the assessment of MSE of conversion errors (see [1-5]). In turn, plots in Fig.4 d-f present the results of similar experiments, but ENOB is measured directly using approach [12, 13].

The presented plots show that IC ADCs have a wide interval of tolerance to DNL errors of pre-converter ADC_{In}. This interval increases for the greater values of ADC_{In} resolution. Under given conditions, the upper boundary ε^* of the tolerance interval [0, ε^*] of DNL intensity values which practically do not change the ENOB, are as follows: for: $N_{ADC} = 2$: $\varepsilon^* \approx 1$, for $N_{ADC} = 4$: $\varepsilon^* \approx 1.3$ and for $N_{ADC} = 8$: $\varepsilon^* \approx 1.4$. Results of the direct ENOB assessment gave the same numerical evaluation of the boundaries of interval [0, ε^*]. However, numerical values of the measured ENOB are some worse than those obtained using its non-direct assessment that requires additional investigation.

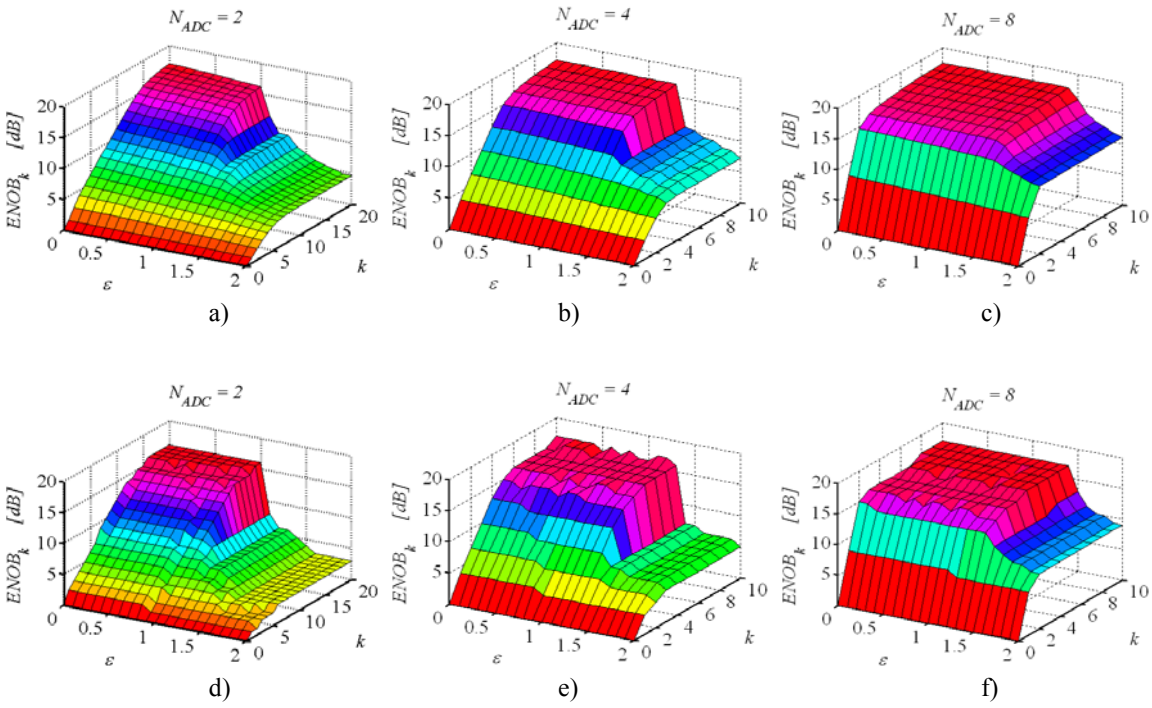

Fig.4. ENOB of IC ADC as a function of cycle number (k) and DNL intensity coefficient (ε) for different values of pre-converter ADC_{In} resolution N_{ADC}.: (a-c) - measured using conventional method, (d-e) - measured directly.

As a supplement to the results of ENOB of IC ADC analysis, empirical plots of SINAD of IC ADC corresponding to the results presented in Fig.4 a-c are presented in Fig.5. The presented plots are obtained in the time domain accordingly to the method proposed in [11]. Corresponding results of assessments in the frequency domain coincide strictly with the results obtained in the time domain.

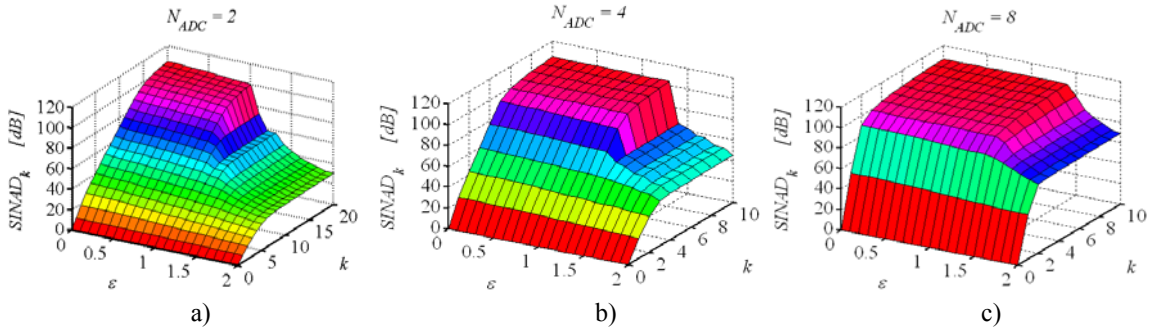

Fig.5. SINAD of IC ADC as a function of cycle number (k) and DNL intensity coefficient (ε) for different values of pre-converter ADC_{In} resolution N_{ADC} (measured using conventional method).

The THD of IC ADC was computed according to [11] under the same conditions as in previous experiments. Corresponding plots are presented in Fig. 6. Both groups of plots in Figs. 4-6 permit to conclude that the DNL of ADC_{In} is not a crucial factor aggravating the performance of IC ADC (and another cyclic ADC). This means that practical implementation of IC ADC can be performed under not too restrictive requirements to their DNL.

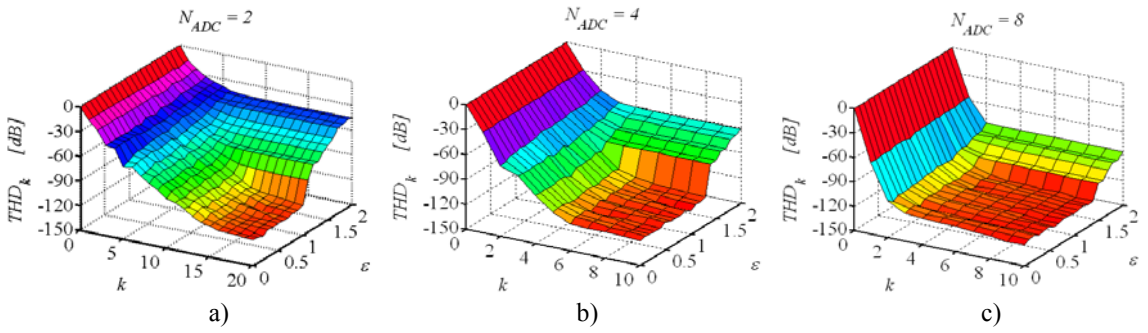

Fig.6. THD of IC ADC as a function of cycle number (k) and DNL intensity coefficient (ε) for different values of pre-converter ADC_{In} resolution N_{ADC}.

In addition to previous experiments, the FFT of the signals converted by IC ADC was analysed depending on the number of cycle for different values of DNL intensity ε, and ADC_{In} resolution $N_{ADC} = 4$. The results of experiments (carried out under the same conditions as before) are presented in Fig. 7, where plots (a)-(c) correspond to the values $\varepsilon = 1$, 1.5, 2, respectively. The obtained results show that the increase of DNL of ADC_{In} transfer function increases the noise floor in FFT plots, but does not cause an appearance of new harmonic components in the spectrum of the converted signal. An increase of ε over the critical value $\varepsilon^* \approx 1.3$ causes abnormal growth of conversion errors, among others due to appearance of missed codes.

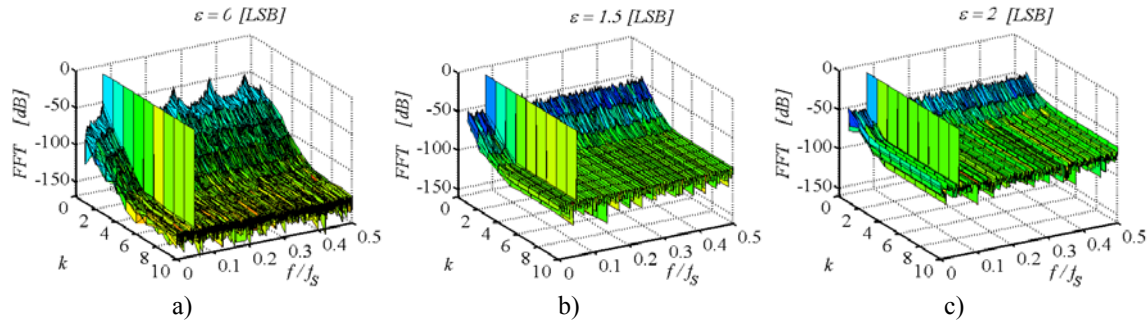

Fig.7. FFT of signal converted by IC ADC as a function of cycle number (k) for different values of DNL errors coefficient (ε) and pre-converter ADC_{In} resolution $N_{ADC} = 4$.

3.2. Integral nonlinearity

The INL of ADC_{In} transfer function was modelled, similarly as in [15], by replacement of the linear approximation of its linear part by a function of the $x^{1+\lambda}$ type

$$f(x) = D\,\mathrm{sgn}(x)\left(\frac{|x|}{D}\right)^{1+\lambda}, \tag{5}$$

where λ determines the intensity of INL (see Fig. 8). In this case, INL (in LSB of ADC_{In}) computed according to [11] has the value:

$$INL_{\max} = 2^{(N_{ADC}-1)}\lambda(1+\lambda)^{-\left(\frac{1+\lambda}{\lambda}\right)}. \qquad (6)$$

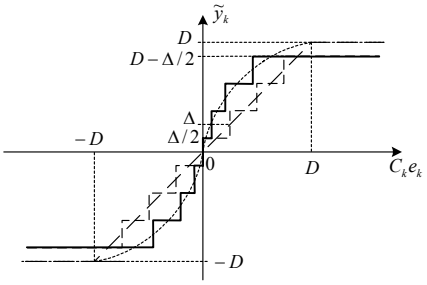

Fig.8. INL error model of pre-converter ADC_{In} transfer function.

The results of simulation assessment of the ENOB dependencies of INL intensity and number of cycles are presented in Fig. 9. As follows from Fig. 9, the admissible range $[-\lambda^*, \lambda^*]$ of the values of λ coefficient which do not influence the IC ADC performance, is as follows: for $N_{ADC} = 2$: $\lambda^* \approx 2.25 \cdot LSB = 1.4063$, for $N_{ADC} = 4$: $\lambda^* \approx 1.5 \cdot LSB = 0.2344$ and for $N_{ADC} = 8$: $\lambda^* \approx 1.5 \cdot LSB = 0.0146$, that corresponds to $INL_{max} = 0.626$ [LSB], $INL_{max} = 0.6186$ [LSB], $INL_{max} = 0.6848$ [LSB] respectively - (in LSB of ADC_{In}). Figure 10 shows corresponding THD plots.

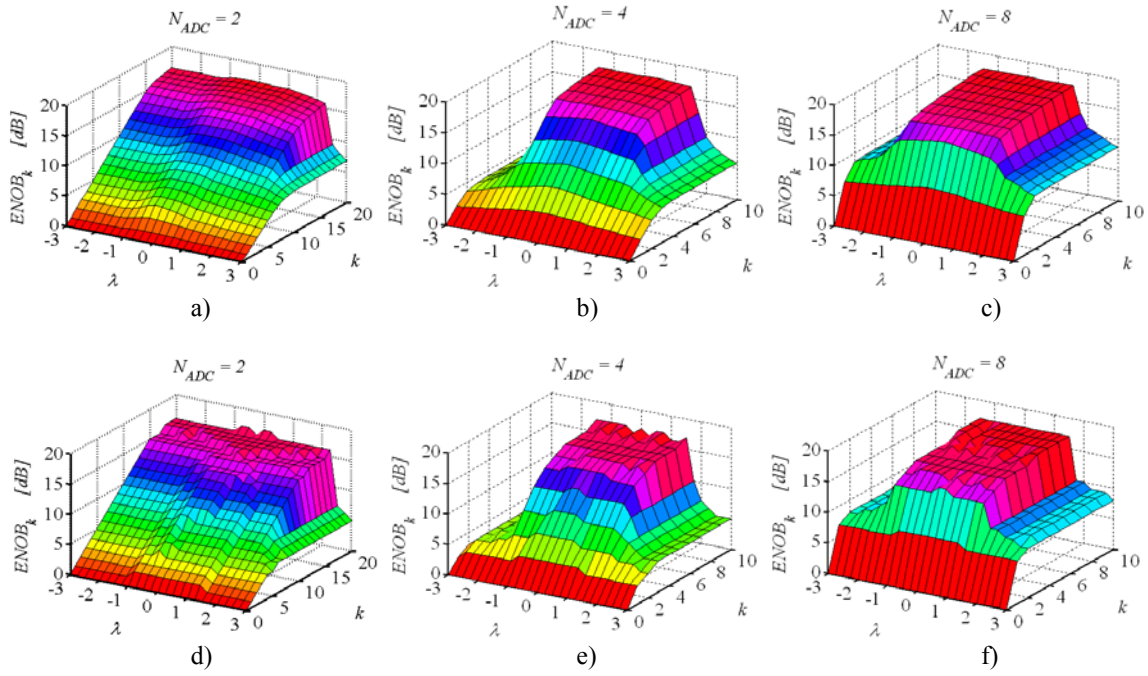

Fig.9. ENOB of IC ADC as a function of cycle number (k) and INL intensity coefficient (λ) for different values of pre-converter ADC_{In} resolution N_{ADC}: (a-c) –measured using conventional method, (d-f) - measured directly.

Analysis of obtained results permits to formulate similar conclusions as formulated in experiments with DNL. In particular, the requirements to INL of ADC_{In} characteristics,

especially to low bit A/D converters $N_{ADC} \leq 8$, can be significantly weakened. Let us note that in many industrial CADCs, 4-bit ADC_{In} are used [7], and requirements to their INL can be significantly weakened as compared to the high-bit converter technology.

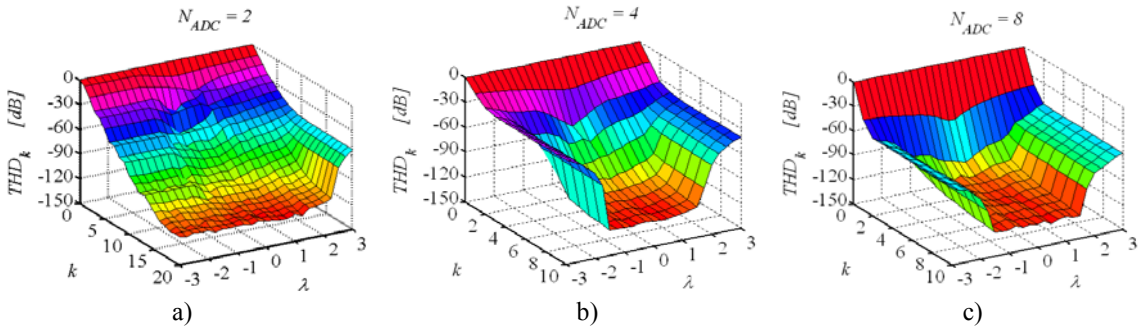

Fig. 10. THD of IC ADC as a function of cycle number (k) and INL errors coefficient (λ) for different values of pre-converter ADC_{In} resolution N_{ADC}.

The FFT plots of signal converted by ICADC as a function of cycle number for different values of the INL intensity λ and the ADC_{In} resolution $N_{ADC} = 4$ are presented in Fig. 11. Contrary to DNL, increase of INL of ADC_{In} over the critical value (under given conditions $\lambda^* \approx 1.5 \cdot LSB = 0.2344$ and $INL_{max} = 0.6186$ [LSB]) results in the appearance of the multiple harmonic components in the spectrum of the signal at IC ADC output.

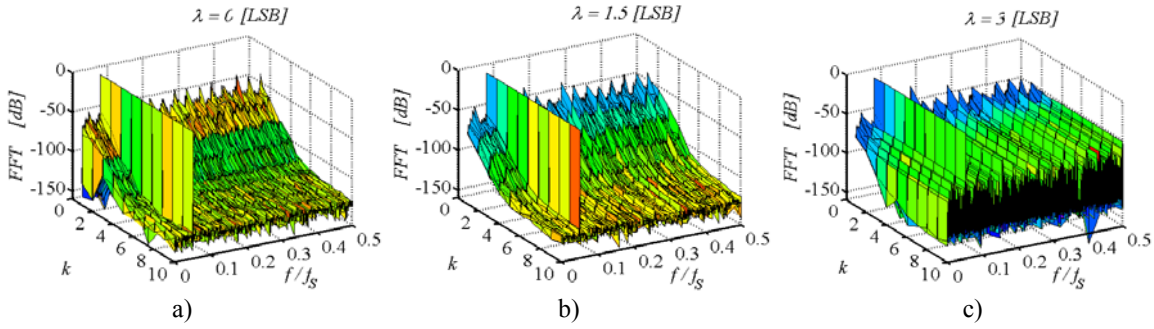

Fig.11. FFT of signal converted by IC ADC as a function of cycle number (k) for different values of INL intensity (λ) and pre-converter ADC_{In} resolution $N_{ADC} = 4$.

4. CONCLUSIONS

The results presented in the paper show that the performance of sub-optimal IC ADCs is resistant to not too large nonlinearities of the transfer function of pre-converter ADC_{In} in IC ADC analogue parts. The empirical values of ENOB, SINAD and THD do not depend, in sufficiently wide intervals of tolerance, on deviations of real characteristics of ADC_{In} from the ideal ones. The model-based method of simulation analysis proposed in the paper permits to assess the boundaries of intervals of tolerance. This, in turn, permits to determine minimal requirements to DNL and INL of ADC_{In} and realize IC ADC using the pre-converters with relatively large DNL and INL that simplifies their production and diminishes the cost of IC ADC.

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ANALIZA WPŁYWU NIELINIOWOŚCI PRZETWORNIKÓW WEWNĘTRZNYCH NA WŁAŚCIWOŚCI INTELIGENTNYCH PRZETWORNIKÓW A/C

Streszczenie

Celem niniejszego artykułu jest zaprezentowanie efektywnego podejścia do ilościowej i jakościowej analizy wpływu nieliniowości wewnętrznych przetworników ADC_{In} na jakość pracy sub-optymalnych cyklicznych przetworników analogowo cyfrowych (IC ADC) należących do nowej klasy przetworników A/C zaproponowanych i badanych w [1-5, 12, 13] i innych pracach. Wyniki przeprowadzonych badań pokazują, że w pewnym zakresie odchylenia charakterystyki przejściowej wewnętrznych przetworników ADC_{In} od jej nominalnej postaci (w przedstawionych eksperymentach do około 0.6-0.7 [LSB] w zależności od rozdzielczości przetwornika) nie wpływają na jakość pracy sub-optymalnych IC ADC. Eksperymenty potwierdziły stabilność empirycznych wartości ENOB, THD, SINAD w dość szerokim zakresie zmian całkowitej i różnicowej nieliniowości ADC_{In}. Zaproponowana w pracy metoda analizy symulacyjnej pozwala na ocenę granic odpowiednich przedziałów

tolerancji, co z kolei pozwala obniżyć wymagania technologiczne oraz obniżyć koszty produkcji wewnętrznych przetworników ADC_{In}, a co za tym idzie obniża ogólne koszty produkcji IC ADC.